Jared Smolens

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Objective

Seeking an experienced/technical lead position in systems performance/power modeling or software optimization.

My recent specializations are in the modeling and design of state-of-the-art processor core and memory subsystem microarchitectures. I led multiple successful products from initial design conception through post-silicon performance tuning and supported post-release customer escalations.

Experience

Oracle America (was Sun Microsystems), Santa Clara, CA.

Senior Principal Software Engineer, Architecture Technology Group
Jan 2008 – present

- Primary duties: Processor core and SoC performance and modeling for SPARC server processors, design space exploration, investigation of potential microarchitectural hardware enhancements and providing timely feedback to RTL designers to make implementation decisions and drive design changes
    - Correlated performance models consistently achieved accuracy within 2% geomean on SPEC CPU 2006 and 5% on full-socket commercial workloads (e.g., SPECjbb, TPC-C)
    - Selected improvements: drove effort to accelerate system call performance by >2x, proposed additional instructions (e.g., CBcond) which have a material impact on performance, MMU hardware tablewalk prediction mechanisms, development and analysis of "thread hog" mechanisms which allow dynamic sharing of out-of-order core resources across multiple threads, identified depreciated opcodes and inefficient code sequences in systems software, analyzed the microarchitectural impacts of virtualization
    - Shipping products: SPARC T4, T5, M5, M6, T7, M7, S7, and several others "in the pipeline"
- Technical lead for:
    - T7/M7/S7 core generation performance model
    - Power modeling effort using performance models; worked with engineers in RTL, circuits, and power management software/firmware to evaluate power-performance tradeoffs
    - Core-side effort to correlate performance model with RTL
- Set performance expectations and helped with post-silicon performance analysis and software tuning, including providing TOIs and support for compiler and operating systems engineers
- Performed workload tracing and analysis
- Developed performance correlation methodology using FSDB/VCD waveform debug to ensure that the performance model maintains near-cycle-accurate behavior with respect to RTL
- Championed regular model regressions, code review process
- Mentored junior engineers

- Advised the development of tools for estimating soft error architectural vulnerability factors (AVF) in performance models and statistical fault injection in RTL for a SPARC processor
- Participated in a working group that defines the next generation SPARC ISA
- Four issued US patents, three US patent applications pending

Carnegie Mellon University, Department of ECE, Pittsburgh, PA

Graduate Research Assistant
August 2002 – December 2007

Major Research Activities:

- Reliable microarchitectures and systems
  - Developed a formal execution model for complexity-effective redundant execution and evaluated a chip multiprocessor-based implementation in simulation; identified and isolated the primary performance factors in redundant multithreaded cores, proposed microarchitecture changes to recover performance; proposed designs for reliable multiprocessor systems
- Hardware design
  - Demonstrated proof-of-concept fingerprint detection with fault injection in a commercial synthesizable Verilog CPU (Sun OpenSPARC)
- Performance modeling
  - Designed and implemented the CMP cache coherence protocol and switch-based network simulator for Flexus, an open-source timing simulator used by architects at Carnegie Mellon and outside institutions (http://www.ece.cmu.edu/~simflex)

Intel Corporation, Santa Clara, CA

Graduate Intern, Test Technology Research Group
Summer 2005

- Modeled and evaluated architectural fingerprints for soft error detection and manufacturing test applications on full-chip Yonah (mobile IA-32 core) RTL
- Investigated implementations of architectural fingerprints on Cedarmill (server IA-32 core) and Montecito (server Itanium core) RTL models

Unisys Corporation, Malvern, PA

Technical Intern, Systems Analysis Modeling and Measurement Group
Summer 1999, Winter 1999 - Spring 2003

- Responsible for writing, documenting and maintaining a multiprocessor cache simulator
- Performed collection and analysis of memory address traces for TPC-C workloads on mainframes for input to a detailed performance queuing model
- Performed initial architectural design, modeling and evaluation of coherence protocol optimizations for migratory sharing in commercial workloads

Education

Carnegie Mellon University, Pittsburgh, PA

Ph.D in in Electrical and Computer Engineering, Aug 2002 - Dec 2007

Recipient of the A. G. Jordan Award for academic excellence and exceptional service, May 2008
Research interests: Microarchitecture and multiprocessor architecture, performance, reliability
Thesis Title: Fingerprinting: Hash-Based Error Detection in Microprocessors
Advisor: Professor James C. Hoe

Carnegie Mellon University, Pittsburgh, PA

Master of Science in Electrical and Computer Engineering, Aug 2001 – May 2002

Carnegie Mellon University, Pittsburgh, PA

Bachelor of Science in Electrical and Computer Engineering, Aug 1997 – May 2001
With University Honors
Relevant Coursework: Advanced Computer Architecture, Multiprocessor Architecture, Hardware Systems Engineering, Dependable Systems Design, Computer Networks, Optimizing Compilers, Database System Design and Implementation

Teaching

- 18-347, 18-447: Introduction to Computer Architecture (Fall 2003, Fall 2004)
  Lead TA, developed and supervised semester-long superscalar RTL processor project.
  40 students and three TAs. Instructor evaluation rating 4.73/5.00 for F03.
  20 students and three TAs. Individual instructor evaluation rating N/A for F04.

- 18-545: Advanced Digital Design Project (Spring 2002)
  Project TA, supervised groups in a semester-long FPGA-based MP3 decoder design project.
  60 students and three TAs. Instructor evaluation rating 4.75/5.00.

- 18-349: Introduction to Embedded Systems (Fall 2001)
  Project TA, supervised labs and revised lab projects, performed grading.
  90 students and five TAs. Instructor evaluation rating 4.95/5.00.

Publications

How the SPARC T4 Processor Optimizes Throughput Capacity: A Case Study
R van Der Pas, JC Smolens
Oracle Whitepaper, April 2012

Fingerprinting: Hash-Based Error Detection in Microprocessors
Ph.D. Thesis, December 2007

PAI: A *Lightweight Mechanism for Single-Node Memory Recovery in DSM Servers*
J Kim, JC Smolens, B Falsafi, JC Hoe
13th Annual Pacific Rim Dependability Conference, December 2007

Detecting Emerging Wearout Faults
JC Smolens, BT Gold, JC Hoe, B Falsafi, K Mai
The Third IEEE Workshop On Silicon Errors in Logic - System Effects (SELSE-3), April 2007

Fingerprinting Across On-Chip Memory Interconnects (poster)
S Chellapa, F deMesmey, JC Smolens, B Falsafi, JC Hoe, K Mai
The Third IEEE Workshop On Silicon Errors in Logic - System Effects (SELSE-3), April 2007

Reunion: Complexity-Effective Multicore Redundancy
JC Smolens, BT Gold, B Falsafi, JC Hoe
ACM/IEEE International Symposium on Microarchitecture (MICRO-39), December 2006

The Granularity of Soft-Error Containment in Shared-Memory Multiprocessors (poster)
BT Gold, JC Smolens, B Falsafi, JC Hoe
The Second IEEE Workshop On System Effects of Logic Soft Errors (SELSE-2), April 2006

TRUSS: A Reliable, Scalable Server Architecture
BT Gold, J Kim, JC Smolens, ES Chung, V Liaskovitis, E Nurvitadhi, B Falsafi, JC Hoe, and AG Nowatzyk
IEEE Micro Special Issue: Reliability-Aware Microarchitectures, November - December 2005

Understanding the Performance of Concurrent Error Detecting Superscalar Microarchitectures
JC Smolens, J Kim, JC Hoe, and B Falsafi
IEEE International Symposium on Signal Processing and Information Technology, Invited Paper, December 2005

Fingerprinting: Bounding Soft-Error Detection Latency and Bandwidth
JC Smolens, BT Gold, J Kim, B Falsafi, JC Hoe, and AG Nowatzyk
IEEE Micro, Top Picks from Computer Architecture Conferences, November - December 2004

Efficient Resource Sharing in Concurrent Error Detecting Superscalar Microarchitectures
JC Smolens, J Kim, JC Hoe, and B Falsafi
ACM/IEEE International Symposium on Microarchitecture (MICRO-37), December 2004

Fingerprinting: Bounding Soft-Error Detection Latency and Bandwidth
JC Smolens, BT Gold, J Kim, B Falsafi, JC Hoe, and AG Nowatzyk
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-11), October 2004

Talks

Code Analysis Tools for Achieving Consistent, Secure, and Reliable Product Quality}
S Lobo, JC Smolens
Oracle OpenWorld, San Francisco, CA. September 2014

Performance Modeling and the SPARC Hardware Design Process
JC Smolens
Oracle Product Architecture Community (Oracle Internal), Redwood Shores, CA. January, 2015

Microarchitectural Power Modeling and How Power Matters to You
JC Smolens
Systems Technology Communications Forum (Oracle Internal), Santa Clara, CA, September, 2014

Detecting Emerging Wearout Faults
JC Smolens, BT Gold, JC Hoe, B Falsafi, K Mai
The Third IEEE Workshop On Silicon Errors in Logic - System Effects (SELSE-3), Austin, TX. April 2007

Reunion: Complexity-Effective Multicore Redundancy

JC Smolens, BT Gold, B Falsafi, JC Hoe
ACM/IEEE International Symposium on Microarchitecture (MICRO-39), Orlando, FL. December 2006

Understanding the Performance of Concurrent Error Detecting Superscalar Microarchitectures
JC Smolens, J Kim, JC Hoe, and B Falsafi
IEEE International Symposium on Signal Processing and Information Technology, Athens, Greece, December 2005

Fingerprinting: Low-Overhead Error Detection in Microprocessors
JC Smolens, TM Mak, JC Hoe
Intel Corporation, Test Technology Research Group, Santa Clara, CA. September 2005

Architectural State Fingerprinting: Bounding Error Detection Latency and Bandwidth
JC Smolens, TM Mak, JC Hoe
Intel Corporation, Test Technology Research Group, Santa Clara, CA. July 2005

Efficient Resource Sharing in Concurrent Error Detecting Superscalar Microarchitectures
JC Smolens, J Kim, JC Hoe, and B Falsafi
ACM/IEEE International Symposium on Microarchitecture (MICRO-37), Portland, OR. December 2004

Fingerprinting: Bounding Soft-Error Detection Latency and Bandwidth
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-11), Boston, MA. October 2004

Issued Patents

RT Golla, PJ Jordan, JI Barreh, MB Smittle, YC Chou, JC Smolens, "Processor operating mode for mitigating dependency conditions between instructions having different operand sizes.'', U.S. Patent 8,504,805, issued August 6, 2013

YC Chou, JC Smolens, JS Brooks, "Apparatus and method for handling dependency conditions between floating-point instructions.'', U.S. Patent 8,458,444, issued June 4, 2013

YC Chou, JC Smolens, JS Brooks, "Handling dependency conditions between machine instructions.'', U.S. Patent 8,429,636, issued April 23, 2013

JC Smolens, RT Golla, MB Smittle, "Dynamic mitigation of thread hogs on a threaded processor.'', U.S. Patent 8,347,309, issued Jan 1, 2013

Three applications pending.

Skills

Languages: C, C++,, Verilog, assembly (SPARC, x86, some ARM), shell scripting, HTML/PHP/JavaScript
Software: Linux, Windows, Solaris, Synopsys tools, user and system-level programming, system administration
Other/hobbies: Cycling, woodworking, bread baking
Volunteering: Ride Coordinator/Board Member, Almaden Cycle Touring Club (since 2014), Webmaster for annual Tierra Bella Bicycle Tour (since 2015)
US Citizen

Professional Activities

- Technical Program Committee member for MICRO-45, MICRO-47, Extended Program Committee member for ASPLOS 2017
- Reviewer for International Symposium on Computer Architecture (ISCA), ACM/IEEE International Symposium on Microarchitecture (MICRO), IEEE/IFIP International Conference on Dependable Systems and Networks (DSN), International Symposium on High-Performance Computer Architecture (HPCA), IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), IEEE MICRO, ACM Transactions on Architecture and Code Optimization (TACO), IEEE Transactions on Computers (TC), International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), and other conferences and journals.
- Community/open source projects
    - Author and maintainer of the "Architectural Transplant" OpenSPARC community project (http://transplant.sunsource.net)
    - Author of patches to WinVNC (IP-based blocking, Windows domain authentication
    - Maintainer of ezimail (text-based IMAPv4 email client, defunct)
- Member, IEEE

References

Available upon request